UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,882	09/30/2003	Randy B. Osborne	42P16963	8106

8791	7590	10/25/2005

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EXAMINER
SCHLIE, PAUL W

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 10/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/676,882	OSBORNE, RANDY B.
	Examiner	Art Unit	
	Paul W. Schlie	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/30/03*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-22 have been examined.

Drawings

2.   The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "memory device of claim 5, further comprising a separately accessible non-volatile memory from which an indication of ... may be read" as cited in claim 6 should have been correspondingly depicted in figures 1 and 4, or previously excluded, or now canceled from the claims. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the

next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3.   Claims 2 and 5, 20 are objected to because of the following informalities:

As claim 2 is improperly numbered as claim 3, but will be referenced as

being claim 2 within this office action response, as presumed to be intended.

As claim 5 cites being dependent on itself, but will be considered as being

dependent on claim 4 within this office action response, as presumed to be

intended.

As claim 20 cites "providing a memory controller an indication of having

the capability to respond ...", but it's unclear what is "having the capability to

respond ..."; so will be presumed to more clearly read "providing the memory

controller an indication of a memory device having the capability to respond ...".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and
> process of making and using it, in such full, clear, concise, and exact terms as to enable any
> person skilled in the art to which it pertains, or with which it is most nearly connected, to make
> and use the same and shall set forth the best mode contemplated by the inventor of carrying
> out his invention.

5.   Claims 3-6, 13-14, 17-18, 21-22 are rejected under 35 U.S.C. 112, first

paragraph, as failing to comply with the enablement requirement. The claims

contain subject matter not described in the specification in such a way as to

enable one skilled in the art to which it pertains, or with which it is most nearly

connected, to make and/or use the invention.

More specifically, no facility or mechanism has been disclosed to enable an external entity to distinctly program and/or access any state contained within the disclosed "memory device", nor for the device to provide indication of any state within that device, beyond that disclosed to enable access to the storage provisioned within the device itself. Therefore any claim dependant on such an implied capability will not be considered to be sufficiently enabled or obvious to one of ordinary skill in the art.

As per claims 3-6, 13-14, 17-18 no mechanism has been disclosed to enable the programming or an indication to be "readable by another device via a memory bus to which the memory device is coupled", beyond the storage contained within the device itself as depicted within the specification and/or drawings. (As an aside, as typically a currently active row/page is physically implicitly closed upon the activation of another within a conventional DRAM bank because they typically share common bit-lines and sense amps by design, it's not clear that claiming the ability to program it, and/or indicate it's presence is reasonable without correspondingly disclosing a supporting implementation.)

Claim Rejections - 35 USC § 102

6.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7.   Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by

Watanabe (5,463,590).

As per claim 1, Watanabe teaches a memory device comprising: at least

one bank comprised of memory cells organized by rows and columns; control

logic where in response to a row activate command will close a previously open

row, and open the row requested; see column 24 table 1 lines 25-38.

Claim Rejections - 35 USC § 103

8.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for

all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described
> as set forth in section 102 of this title, if the differences between the subject matter sought to
> be patented and the prior art are such that the subject matter as a whole would have been
> obvious at the time the invention was made to a person having ordinary skill in the art to which
> said subject matter pertains. Patentability shall not be negatived by the manner in which the
> invention was made.

9.   Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over

Watanabe (5,463,590) in further in view of Osborne (US App.10/676,882) and

Bondurant et al. (6,330,636).

As per claim 2, Watanabe teaches claim 1 (as above), but does not teach

that data may be transferred across the data bus synchronized to twice the clock

rate of the device. However Osborne acknowledges DDR "Double Data Rate"

DRAM as prior art within the Background of the application, see page 3 lines 16-

18, as is also taught by Bondurant et al. (also teaching that DDR DRAM memory

devices tend to support the mode of operation as in claim 1). Therefore it would

be obvious to one of ordinary skill in the art to combine DDR transfer capabilities

with that taught by Watanabe, to reduce the latency of multi-cycle memory data transactions.

10.   Claims 7-12, 15-16, 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (5,463,590), Osborne (US App.10/676,882) and Bondurant et al. (6,330,636) in further view of "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" second edition, as published 10/2002 in English, and 8/2002 in Japanese, and Schaefer (5,636,173).

As per claims 7-12, 15-16 and 19-20, Watanabe, Osborne and Bondurant et al. teach a controller interconnected with a memory device comprising: at least one bank comprised of memory cells organized by rows and columns; control logic where in response to a row activate command will close a previously open row, and open the row requested, similarly to claims 1-2; however does not teach a computer system comprised of such a memory device, a processor, and memory controller capable of tracking as many as two different storage locations contained within a memory device such that upon a request potentially necessitating the activation of a row, it may be determined if the presence of an open row will corresponding necessitate the closing/pre-charging a currently open row such that all correspondingly required delay timing requirements of the memory device; nor that an auto-pre-charge may be implicitly previously conducted upon a request for a transaction from a row different from the row presently being requested to active . "NEC Preliminary User's Manual, Memory Controller NA85E35, NBA85E535Vxx" teaches a computer system comprising a processor and memory which can determine if a pre-charge command/delay is
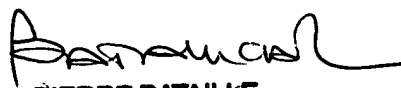
required to be accounted for in response to a request for a memory transaction

from a row which may differ from a previously open row, see pages 22, 26, and

59; and Schaefer teaches a memory bank may be implicitly auto-pre-charged in

response to a row transaction in preparation for a subsequent row activation, see

figure 2 and page 1 abstract lines 10-13. It would have been obvious to one of

ordinary skill in the art to combine these for the benefit of potentially improving

the memory transaction performance and efficiency of such a system.

11.   Any inquiry concerning this communication or earlier communications from

the examiner should be directed to Paul W. Schlie whose telephone number is

571-272-6765. The examiner can normally be reached on Mon-Thu 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the

examiner's supervisor, Matthew Kim can be reached on 517-272-4182. The fax

phone number for the organization where this application or proceeding is

assigned is 571-273-8300.

Information regarding the status of an application may be obtained from

the Patent Application Information Retrieval (PAIR) system. Status information

for published applications may be obtained from either Private PAIR or Public

PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-

free).

PIERRE BATAILLE
PRIMARY EXAMINER